REMARKS

Applicant wishes to thank Examiner Pizarro-Crespo for the time spent during a telephonic interview. During that interview the undersigned remarked that Shimizu was non-analogous/non-related art as it related to chip capacitors, illustrated in Fig. 7, and not integrated circuitry as recited in Applicant's claims. In addition, the undersigned remarked that while Shimizu did not disclose any specific temperatures for forming the disclosed devices, that based on the extremely high values of permittivity supplied, for example in Table 2, that Shimizu must employ very high temperatures for the disclosed process, temperatures that are likely to be incompatible with integrated circuitry. This high temperature processing indicated by Anderson which states "the higher the temperature of polycrystalline film formation the higher the dielectric constant" (col. 3, lines 61-63) and by comparing the dielectric constant given by Anderson for $BaTiO_3$, about 330 when formed at 700°C and in excess of 1000 when formed at about 1000°C to the permittivity given for such material by Shimizu in Table 2, 1,500-2,500.

The Examiner stated that he believed that these remarks were persuasive, but that as he lacked signature authority, he would have to consult with his supervisor. The undersigned asked if he could participate in a three-way conversation to personally present the above remarks and it was agreed that such a meeting would be scheduled by the Examiner. However, in a follow-up telephone conversation, the Examiner suggested that the undersigned submit a formal, written response rather than the previously agreed upon second interview.

Rejection under 35 U.S.C.§103(a)

Anderson in view of Shimizu

Claims 1, 4-9, 11, 13-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson (US 5,390,072) in view of Shimizu (US 4,873,610). Applicant traverses.

Claim 1 recites, in pertinent part, "integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer, the high K substantially amorphous material and the high K substantially crystalline material constituting different chemical compositions." Claims 4-9, 11 and 13-15 depend from Claim 1.

With regard to Anderson, the Examiner admits that such does not show that the amorphous and crystalline layers can constitute materials of different chemical constitutions as recited by Applicant's claim. For this teaching, the Examiner turns to Shimizu which is represented as disclosing an invention where at least two different dielectric materials are employed in a capacitor to provide high permittivity. Applicant notes that permittivity is a physical property of a material, at a given temperature, that is directly related to dielectric constant by the relationship $K=\varepsilon/\varepsilon_0$ where K is dielectric constant and ε and ε_0 are the permittivity of the material and of free space (generally equal to 1), respectively, at any temperature.

From this combination of Anderson with Shimizu, the Examiner concludes that it would have been obvious at the time of the invention for one of ordinary skill in the art to combine the different chemical compositions of Shimizu with the capacitor of Anderson. Applicant DOES NOT AGREE.

As mentioned in the interview summary, Shimizu is non-analogous art with respect to Anderson and to Applicant's claimed invention. Both Applicant and Anderson form a capacitor structure suitable for inclusion in an integrated circuit. Thus both employ processing that is consistent with such circuitry. Shimizu, on the other hand, forms chip capacitors which contain materials having extremely high permittivities. Such chip capacitors having no integrated circuitry formed therewith (see, Fig. 7). Hence the capacitor structure of Shimizu is not analogous to any of the structures formed by either Anderson or the Applicant.

In addition, Anderson teaches that formed at 700°C, $BaTiO_3$ has a dielectric constant of about 330 while forming the same material at 1000°C results in a film having a dielectric constant which may exceed 1000. Thus Anderson shows that the higher the temperature used in the forming of a material, the higher the dielectric constant. Shimizu also forms a capacitor employing $BaTiO_3$. However, as evidenced by Table 2, Shimizu obtains permittivities for such layers of 1500 to 2500, thus indicating use of a temperature likely to be well in excess of the 1000°C taught, but not preferred, by Anderson. Applicant respectfully asserts that Shimizu's high temperature processing is likely to be destructive to integrated circuitry such

as is provided by both Anderson and the Applicant. Hence Shimizu CANNOT be analogous art.

Applicant further asserts that Shimizu is not relevant to either Anderson or Applicant's claimed invention. Shimizu does disclose forming multilayer capacitor structures where the multiple layers have different chemical compositions. Each of Shimizu's disclosed capacitors is formed using ONLY crystalline layers and CANNOT, therefore, be relevant to mixing both amorphous and crystalline layers for forming capacitors. Thus where the Examiner alleges that it would have been obvious to one of ordinary skill in the art to modify Anderson with the layers of different chemical composition disclosed by Shimizu, Applicant asserts such an allegation is incorrect for at least the reasons given above.

Moreover, Anderson discloses (col. 4, lines 46-59), that the capacitance and leakage of his inventive structure is an unexpected result observed while trying to solve the problem of high dissipation factors and leakage current in thin film integrated circuit capacitors. Specifically, Anderson observed that the capacitance is higher and the leakage is lower than what would have been predicted when combining amorphous and crystalline layers of the same material. Shimizu, on the other hand, discloses that his multilayer structures give results that vary from what is expected as a function of layer thickness and that this variation is with regard to the maximum point (compare Fig. 2 to Fig. 3 and col. 3, lines 27-62). It will be noted that Shimizu's focus was on controlling the phase transition temperature to include the maximum permittivity and to eliminate the addition of a shifter or a depressor to the

ceramic materials to simplify the manufacturing process. Shimizu additionally considers multiple layers to reduce dielectric loss caused by pinholes in single layer capacitors (col. 1, lines 42-54). Applicant respectfully asserts, therefore, that where each of the cited art discloses a different unexpected result, while attempting to solve different problems, it cannot be obvious to combine the teachings of such art as alleged by the Examiner.

The Examiner is referred to MPEP: 2141.01(a) which states, citing to *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992), that "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." Applicant has shown that Shimizu is not in the appropriate field of endeavor and that Shimizu and Anderson were focused on solving unrelated problems, hence it is submitted that Applicants asserts that the instant rejection is incorrect is in accordance with §2141.01(a). Such rejection should be withdrawn and Claims 1, 4-9, 11 and 13-15 allowed.

Anderson in view of Shimizu further in view of Ramakrishnan

Claim 10 stands rejected under 35 U.S.C. §103(s) as being unpatentable over Anderson, in view of Shimizu, as applied to Claim 1 above, and further in view of Ramakrishnan (US 5,943,580). Applicant traverses.

Claim 10 depends from Claim 1, hence Applicant's remarks with regard to Anderson and Shimizu above are germane to the instant rejection of Claim 10 and are incorporated herein by reference. With regard to Ramakrishnan, the Examiner presents such art only to show that the additional aspects of

Claim 10 are taught in such cited art. The Examiner does not allege that Ramakrishnan, nor does Ramakrishnan in fact, provide any teaching or suggestion to remedy the deficiencies shown above in the Examiner's combination of Anderson and Shimizu. Therefore, without admission as to what Ramakrishnan might teach or suggest, Applicant respectfully asserts that Claim 10 is allowable at least for the same reasons as is Claim 1.

Anderson in view of Shimizu further in view of Graettinger

Claims 12 and 16 stand rejected under 35 U.S.C. §103(s) as being unpatentable over Anderson, in view of Shimizu, as applied to claim 1 above, and further in view of Graettinger (US 5,844,771). Applicant traverses.

Claims 12 and 16 depend from Claim 1, hence Applicant's remarks with regard to Anderson and Shimizu above are germane to the instant rejection of such claims and are incorporated herein by reference. With regard to Graettinger, the Examiner presents such art only to show that the additional aspects of Claims 12 and 16 are taught or suggested by such cited art. The Examiner does not allege that Graettinger, nor does Graettinger in fact, provide any teaching or suggestion to remedy the deficiencies shown above in the Examiner's combination of Anderson and Shimizu. Therefore, without admission as to what Graettinger might teach or suggest, Applicant respectfully asserts that Claims 12 and 16 are allowable at least for the same reasons as is Claim 1.

In summary, Applicant having responded to each of the rejections and objections, respectfully asserts that Claims 1 and 4-16 are in condition for allowance. Action to that effect is earnestly sought. If, however the

Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: July 25, 2001

By: _____
Bernard Berman
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/512,149
Filing Date ..... February 20, 2000
Inventor ..... Vishnu K. Agarwal
Assignee ..... Micron Technology, Inc.
Group Art Unit 2814
Examiner ..... M. Pizarro Crespo
Attorney's Docket No. MI22-1322
Title: Integrated Circuitry Including a Capacitor With an Amorphous and a Crystalline High K Capacitor Dieletric Region (As Amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO MAY 2, 2001 OFFICE ACTION

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

None.